

What is claimed is:

1. A multi-layer integrated semiconductor structure, comprising:
  - at least a first device layer including a first plurality of semiconductor elements;
  - a first insulating layer disposed over the first device layer and including at least a first via-hole;
  - a first conductive plug disposed in the first via-hole;
  - a first interface portion disposed over at least a portion of the first conductive plug;
  - at least a second device layer including a second plurality of semiconductor elements and including a second via-hole; and
  - a second conductive plug disposed in the second via-hole, wherein the second device layer is coupled to the first device layer via the first interface portion and wherein the first interface portion provides a communication relationship between the first device layer and the second device layer.
2. The multi-layer integrated semiconductor structure of claim 1 further comprising a first conductive interconnect element disposed in the first insulating layer and wherein the first via-hole is provided in the first insulating layer to expose at least a portion of the first conductive interconnect element.
3. The multi-layer integrated semiconductor structure of claim 2, wherein the first conductive plug includes a first end coupled to the first conductive interconnect element and a second end coupled to the first interface portion.
4. The multi-layer integrated semiconductor structure of claim 3, wherein the second via-hole is formed on a bottom surface of the second device layer and exposes a portion of at least one element of the second plurality of semiconductor elements.

5. The multi-layer integrated semiconductor structure of claim 1, wherein the second via-hole is formed on a top surface of the second device layer and exposes a portion of at least one element of the second plurality of semiconductor elements.
6. The multi-layer integrated semiconductor structure of claim 5, wherein the second conductive plug includes a first end coupled to at least one element of the second plurality of semiconductor elements and a second end coupled to at least a portion of a second interface portion disposed on the top surface of the second device layer.
7. The multi-layer integrated semiconductor structure of claim 4, wherein the second conductive plug includes a first end coupled to the at least one element of the second plurality of semiconductor elements and a second end coupled to the first interface portion.
8. The multi-layer integrated semiconductor structure of claim 3, wherein the second via-hole is formed on a bottom surface of the second device layer and exposes a portion of a second conductive interconnect.
9. The multi-layer integrated semiconductor structure of claim 8, wherein the second conductive plug includes a first end coupled to the second conductive interconnect and a second end coupled to the first interface portion.
10. The multi-layer integrated semiconductor structure of claim 3, wherein the second via-hole is formed on a top surface of the second device layer and exposes a portion of at least a second conductive interconnect.
11. The multi-layer integrated semiconductor structure of claim 10, wherein the second conductive plug includes a first end coupled to the second conductive interconnect and a second end coupled to at least a portion of a second interface portion disposed on the top surface of the second device layer.

12. The multi-layer integrated semiconductor structure of claim 1, wherein the first via-hole exposes a portion of at least one element of the first plurality of semiconductor elements.
13. The multi-layer integrated semiconductor structure of claim 12, wherein the first conductive plug includes a first end coupled to the at least one element of the first plurality of semiconductor elements and a second end coupled to the first interface portion.
14. The multi-layer integrated semiconductor structure of claim 1, wherein the first interface portion includes a conductive material.
15. The multi-layer integrated semiconductor structure of claim 14, further including a second interface portion disposed between the first and second device layers.
16. The multi-layer integrated semiconductor structure of claim 15, wherein the second interface portion includes an adhesive material.
17. A multi-layer integrated semiconductor structure, comprising:
  - at least a first device layer including at least a first doped semiconductor region;
  - a first insulating layer disposed over the first device layer and including at least a first via-hole;
  - a first conductive material disposed in the first via-hole;
  - an interface portion disposed over at least the first conductive material;
  - at least a second device layer including at least a second doped semiconductor region and including a second via-hole; and
  - a second conductive material disposed in the second via-hole, wherein the second device layer is coupled to the first device layer via the interface portion and wherein the interface portion provides a communication relationship between the first device layer and the second device layer.

18. The multi-layer integrated semiconductor structure of claim 17 further comprising a first conductive interconnect element disposed in the first insulating layer and wherein the first via-hole is formed on the first insulating layer and exposes at least a portion of the first conductive interconnect element.
19. The multi-layer integrated semiconductor structure of claim 18, wherein the first conductive material includes a first end coupled to the first conductive interconnect element and a second end coupled to the interface portion.
20. The multi-layer integrated semiconductor structure of claim 17, wherein the second via-hole is formed on a bottom surface of the second device layer and exposes a portion of the second doped semiconductor region.
21. The multi-layer integrated semiconductor structure of claim 17, wherein the second via-hole is formed on a top surface of the second device layer and exposes a portion of the second doped semiconductor region.
22. The multi-layer integrated semiconductor structure of claim 21, wherein the second conductive material includes a first end coupled to the second doped semiconductor region and a second end coupled to another interface portion disposed on the top surface of the second device layer.
23. The multi-layer integrated semiconductor structure of claim 17, wherein the second via-hole is formed on a bottom surface of the second device layer and exposes a portion of a first conductive interconnect.
24. The multi-layer integrated semiconductor structure of claim 23, wherein the second conductive material includes a first end coupled to the first conductive interconnect and a second end coupled to the interface portion.
25. The multi-layer integrated semiconductor structure of claim 17, wherein the first via-hole exposes a portion of the first doped semiconductor region.

26. The multi-layer integrated semiconductor structure of claim 25, wherein the first conductive material includes a first end coupled to the first doped semiconductor region and a second end coupled to the interface portion.
27. The multi-layer integrated semiconductor structure of claim 17, wherein the interface portion includes a conductive material.
28. The multi-layer integrated semiconductor structure of claim 17, wherein the first conductive material includes a first conductive plug.
29. The multi-layer integrated semiconductor structure of claim 17, wherein the second conductive material includes a second conductive plug.
30. The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer is constructed and arranged to operate using at least one of electronic components, optical components or micro-electromechanical components.
31. The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer is constructed and arranged to operate using at least one of electronic components, optical components or micro-electromechanical components.
32. The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes at least one die element.
33. The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer includes at least one die element.
34. The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes at least one die element of a plurality of die elements located on a semiconductor wafer.

35. The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer includes at least one die element of a plurality of die elements located on a semiconductor wafer.
36. The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area whereby the first predetermined surface area differs from the second predetermined surface area.
37. The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area whereby the first predetermined surface area is substantially equivalent to the second predetermined surface area.
38. The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes a first predetermined geometry.
39. The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer includes a second predetermined geometry.
40. A multi-layer semiconductor structure, comprising:  
a semiconductor wafer including a plurality of semiconductor structures each of which includes a plurality of semiconductor elements;  
at least a first conductive bonding interface segment disposed over at least a first semiconductor structure of the plurality of semiconductor structures of the semiconductor wafer and being in an electrical communication relationship with at least a first semiconductor element of the first semiconductor structure;  
at least a second semiconductor structure including a plurality of semiconductor elements being coupled to the first semiconductor structure via the first conductive bonding interface segment, wherein the first conductive bonding interface segment is in an electrical communication relationship with at least a second semiconductor element of

the plurality of semiconductor elements of the second semiconductor structure for permitting at least the first semiconductor element of the first semiconductor structure to communicate with at least the second semiconductor element of the second semiconductor structure, via the first conductive bonding interface segment.

41. A multi-layer semiconductor structure, comprising:

- at least a first semiconductor structure including a first plurality of conductive elements;

- a plurality of conductive bonding interface segments disposed over the first semiconductor structure and each being in an electrical communication relationship with one or more of the conductive elements of the first semiconductor structure;

- at least a second semiconductor structure including a second plurality of conductive elements and being coupled to the first semiconductor structure via at least a first segment of the plurality of conductive bonding interface segments;

- at least a third semiconductor structure including a third plurality of conductive elements and being coupled to the first semiconductor structure via at least a second segment of the plurality of conductive bonding interface segments, wherein the first plurality of conductive elements of the first semiconductor structure, the second plurality of conductive elements of the second semiconductor structure and the third plurality of conductive elements of the third semiconductor structure are constructed and arranged to inter communicate via the first and second segments of the plurality of conductive bonding interface segments.